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Integrated High-Temperature Isolation barrier with Coreless Transformer

Rémi Perrin, Bruno Allard, Christian Martin, Cyril Buttay, Université de Lyon, Ampere, INSA de Lyon, UCB Lyon 1, Lyon, France

Abstract

A novel coreless technology based on an existing process but initially designed to produce integrated passive components for commercial temperatures, is used and its capability at 200 C is tested. Design aspects and electrical characterizations of the samples are presented. An endurance test, realized with a full modulation and demodulation prototype board, shows a satisfactory behaviour at high temperatures. Finally, a dynamic isolation test checks the coreless transformer behaviour against dV/dt perturbation. This work targets a high-temperature inverter application with high-frequency switching frequency and based on multi-chip module.

1 Introduction

The trend of electrification in Aerospace applications requires both high temperature and high frequency operation to achieve high power density for the future power converters [1]. This implies that power modules in such converters need to operate at very high ambient temperatures, e.g. $200-250\,^{\circ}\mathrm{C}$, interconnectors parasitic must be as low as possible, switching frequencies are in the 20 kHz to 500 kHz range. Moreover, the GaN technology has emerged as promising for high frequency, high efficiency and high-density power conversion due to a better figure of merit than comparable Si and SiC transistors. A larger number of GaN devices have been manufactured for a large field of applications from low power voltage regulators to high power infrastructure base-stations [7]. The switching frequency is continuously increasing to reduce the size of passive components and to increase power density. dV/dt increase imposes the choice of effective isolation barrier to the control signal lines. The work presented in this paper aims to deliver a functional prototype control signal isolation for high-temperature ambient application. Design and test of the prototype are targeted for aerospace specifications.

2 Coreless transformer for insulation of control signals in a high temperature inverter leg

Recent advances have brought to industrial level the coreless technology for the insulation of control signals in an integrated driver chip [5-6]. There is an interest to develop a discrete coreless transformer. In fact, discrete components require less development efforts than fully integrated systems and permits flexibility in various applications for example in Fig. 1.

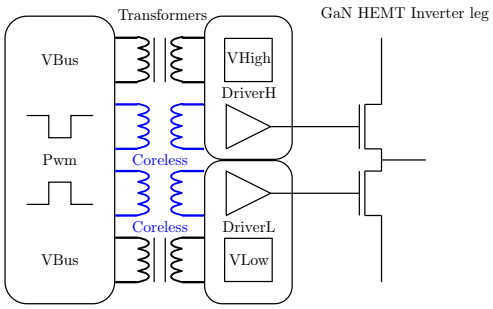

Figure 1 *Bloc diagram of an integrated inverter leg with coreless transformers for control isolation.*

3 Coreless technology

In Fig. 2 coreless transformers are processed using Integrated Passive Device technology (IPD) from STMicroelectronics. It consists of a glass wafer onto which two layers of copper are placed, insulated by a specific resin. It should be noted that the resin is a broad band-sensitive photopolymer named B-staged bisbenzocyclobutene (BCB). It is intended to be used as dielectrics in thin film microelectronics applications. This polymer was not specially developed for high temperature applications, however the process of reticulation that happens during the initial curing process leads to believe that an extension of the usual temperature limit ($125 to 175\,^{\circ}\mathrm{C}$) is achievable.

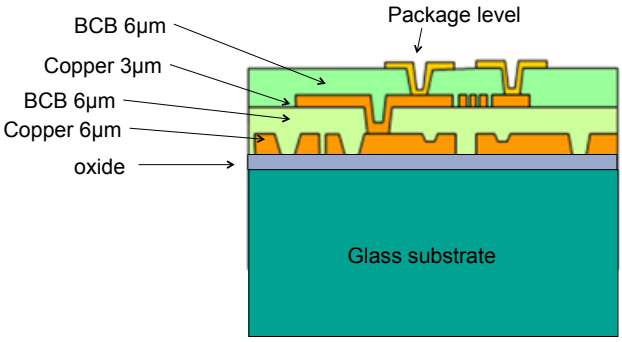

Figure 2 *Simplified cross section of the technology used for the coreless transformer. With Courtesy of STMicroelectronics*

4 Electrical characterization

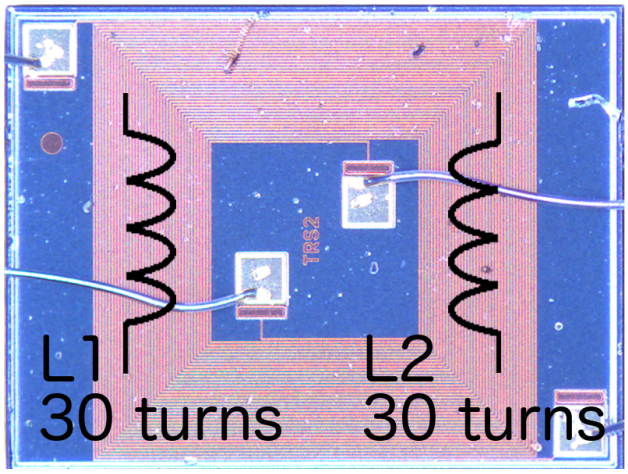

Figure 3 *Picture with schematic of a TRS2 coreless transformer.*

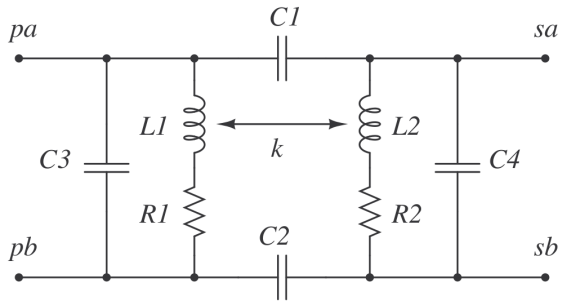

Figure 4 *Electrical model of the coreless transformer with parameters value in Tab. 1*

For the purpose of verification the transformer is characterized using an impedance analyzer against the model in Fig. 4. On a practical point of view, there is no interest in reducing the operating frequency of the transformer

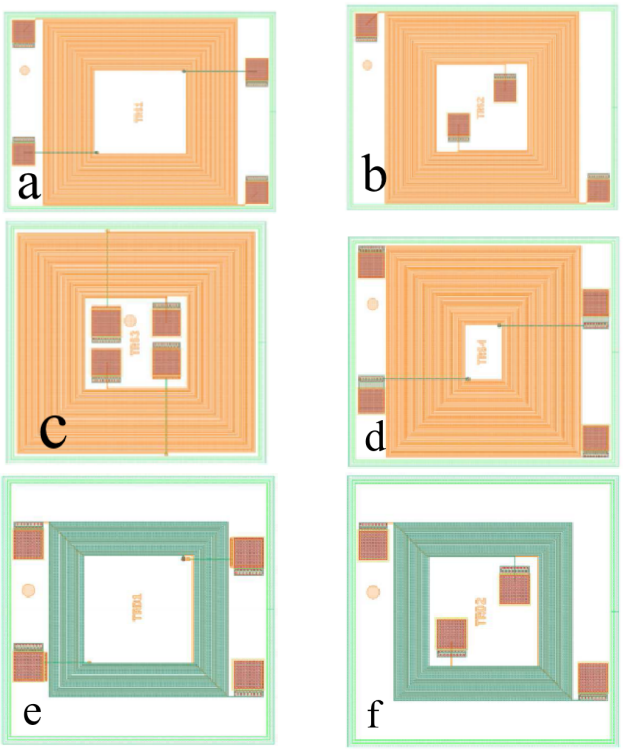

Figure 5 *Coreless transformer structures (a)TRS1 (b)TRS2 (c)TRS3 (d)TRS4 (e)TRD1 (f)TRD2*

Fig. 3. On the contrary an increase in the carrier frequency is needed to reduce the coil driving current and to reduce the physical dimensions. The upper frequency limit for the transformer is set by the parasitic capacitances and the coil inductance what defines a self-resonant frequency. The other limiting factor for the high frequencies is the ability of the transceiver to source and sink current at high frequency. The coils are measured by an impedance analyzer and matched to a simple equivalent circuit model because it is well adapted to low frequency, lower than 100 MHz.

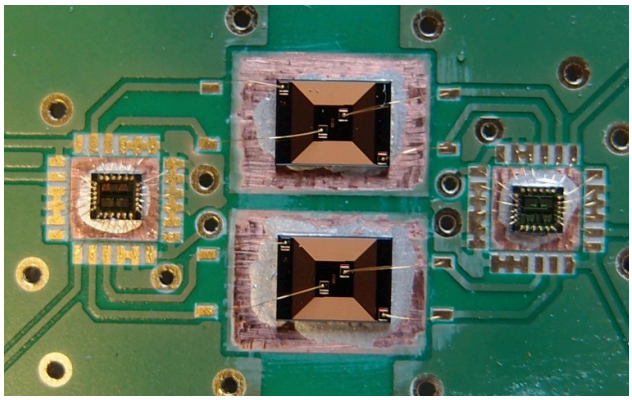

Figure 6 *Coreless Isolated board with two Xrel XTR40010 Transceiver for dual channel isolated lines*

Table 1 *Parameter values from frequency domain measurements on demonstrators in Fig.5*

	L1/L2 [uH]	R1 [Ohm]	R2 [Ohm]	k	Lf [uH]	C1/C2 [pF]
TRS1	0.966	47.753	46.654	0.923	0.142	14.6
TRS2	0.958	49.892	49.928	0.922	0.144	14.5
TRS3	0.932	51.791	51.789	0.920	0.142	13.2
TRS4	1.006	50.872	50.422	0.924	0.147	14.5
TRD1	1.018	40.862	39.888	0.933	0.132	7.6
TRD2	1.007	39.204	40.222	0.933	0.131	7.5

5 High-Temperature Isolation Board Design

Different coreless transformer structures have been fabricated to find the optimal winding and pads location structure Fig. 5. The primary winding and the secondary winding are etched on the same metal level, while the second metal level is used to "bring back" the extremity of the coil from the center of the device to the side of the chip. For some applications it is necessary to have the contact pads at the corner of the chip, for improving insulation at package level for example. This implementation is called "single layer" transformer and is noted "TRS". It was chosen over a double layer structure because the dielectric isolation is the features better performances.

In Figs. 6 and 7 two XTR40010 SOI modulation chips

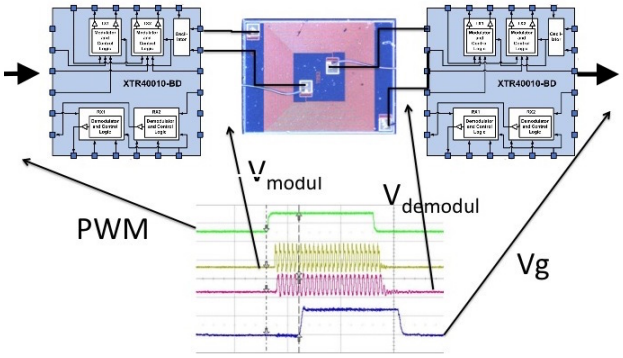

Figure 7 *Modulation and demodulation principe with two Xrel XTR40010 Transceiver*

modulate the PWM signal in high-frequency (25 MHz) to transfer the signal through the coreless transformer. The second chip makes the opposite. The active area is around $0.3in^2$. And the first test gives a transmission delay of 90 ns (@200°C), that fixes a switching frequency limit at 11 MHz for the global inverter system. This value is more than enough to reach the 500 kHz operating frequency target.

5.1 Board Aging Test

This 600 hour aging test has been performed with the coreless board (Fig. 8) at a constant temperature of 200°C. This allows to see the impact of the coreless structure at

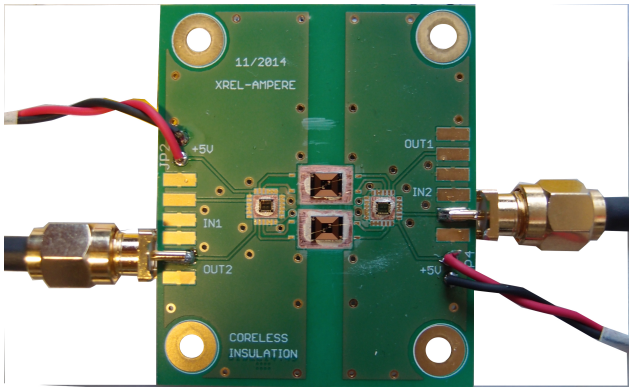

Figure 8 *Coreless Isolated board under testing*

high temperature on the global system robustness. An automatic measurement system tests every 30 minutes the input/output consumption and the input/output frequency. The current consumption variation is less than 5 uA. The Fig. 9 shows the jitter in percent between the input and the output frequency, the error is limited by the multimeter resolution. This test allows to see that the ageing issues men-

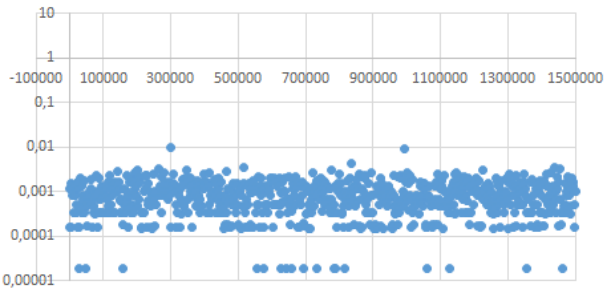

Figure 9 *Input/output frequency error in percent*

tionned in [4,7] for the coreless structure has no impact on the final application. The accuracy and the stability of the global function reach the required specifications.

5.2 Dynamic Isolation Test

In order to check the dynamic isolation of the barrier a dV/dt setup was built at the lab. The dV/dt generator allows a dV/dt variation between 5 to 100 kV/us. By connected the generator between the ground and the DUT reference,

it allows to reproduce the perturbation generate by a phase leg. A probe is connected at the output of the demodulator in order to control the logic state.

In Fig. 11, the principle of the test is to control the output logic state when DUT is disturbed by dV/dt. Fig. 10 shows a spike on the logic signal forced by the dV/dt. The final result, shows a limit of 65 kV/us of the board with a TRS2 coreless transformer and a distance between board and ground of 2 cm (0.065 in). This limit may explain by the current limitation of the modulator-demodulator chip output buffer. The common mode current generate by a 65 kV/us dV/dt through a 14 pF transformer capacitance reaches the maximum allowed by the SOI chip buffer. A final test with the board in a complete phase leg drive system will be done to take in count all the interaction.

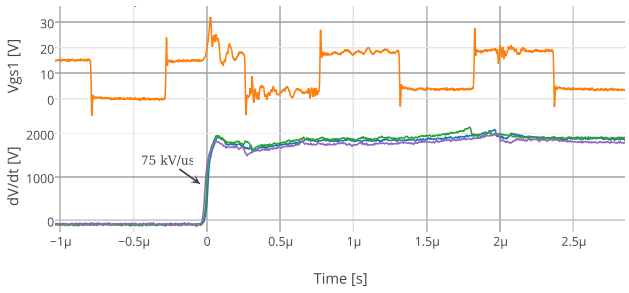

Figure 10 *75 kV/us dV/dt perturbation on a PWM logic signal*

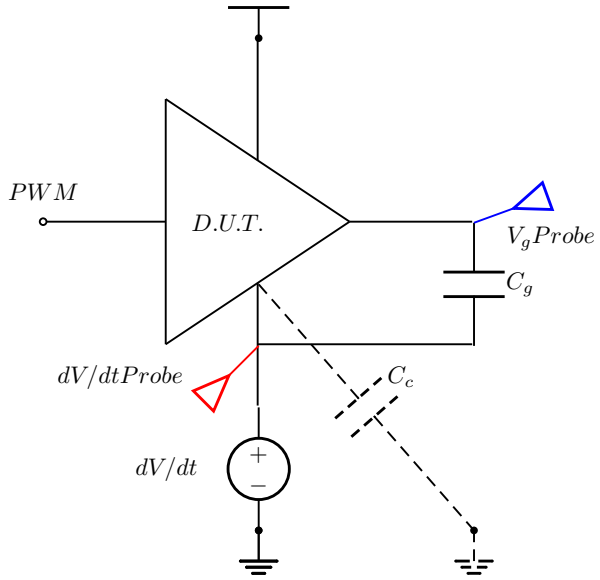

Figure 11 *Schematic of the dV/dt generator connected to the coreless transformer board, Cc is the coupling capacitor between board and ground*

6 Conclusion

A specific integrated coreless component was designed and fabricated using an industrial production process. It was characterized using a specific simplified model. An integrated setup test is designed to realize advanced isolation tests in a large temperature range. Primary functional tests give good results. Ageing tests prove those coreless transformers are interesting for a high-temperature isolation barrier in high dV/dt environment.

7 Literature

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