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Evaluation of the PCB-embedding technology for a 3.3 kW converter

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Abstract—This paper presents a converter fully made using PCB embedding technology (including the semiconductor devices, but also their gate driver circuits as well as the passive components). This converter is rated at a high-power (3.3 kW) considering the PCB technology. Here, the focus is given to the experimental validation of the embedding process, with the characterization of many of the embedded devices (SiC MOS-FETs, diodes, capacitors). These results show that most of the components were unaffected by the process, with the noticeable exception of the large inductors which exhibit variations in the inductance values as well as a large ac resistance. Finally, the converter is successfully assembled and tested at low power.

I. INTRODUCTION

This article presents the implementation of a 3.3 kW, bidirectional, ac/dc converter which could be used, for example, as part of an on-board battery charger in an electric vehicle (in this case, the bidirectional energy transfer capability could be used for vehicle-to-grid [1]). The circuit design of this converter is presented in [2]. Here, we focus on the integration technology used to actually build the converter: PCB embedding.

Embedding components within a Printed Circuit Board (PCB) is a relatively recent technology [3]. It is particularly attractive for power applications, as it allows to reduce the inductance of the interconnects or to provide better cooling. Detailed reviews of this technology are given in [4], [5]. It consists in inserting components in the material stack used to form multi-layer PCBs, prior to the lamination process. Afterwards, connections are formed with the embedded components using microvias (laser-drilled holes filled with electroplated copper).

Semiconductor chips are especially good candidates for embedding, because they experience the fastest current changes and the highest power density in a converter. In [6], the authors present the embedding of SiC power dies. Thermal performance is increased through the use of ceramic or thick copper layers. Regarding circuit parasitics, a very low value of loop inductance (0.43 nH) is achieved to connect GaN transistors in [7], thanks to PCB embedding. Many other publications on this topic are listed in [5].

Beyond power semiconductors, it may be interesting to embed other components. In particular, magnetic components can be made by embedding a solid ferrite core [8], some ferrite powder [9] or thin sheets of amorphous magnetic materials [10]. Windings are then formed by patterning the copper

layers of the PCB and drilling vias. In some cases, sheets of polymer loaded with magnetic particles can directly be laminated as part of a multilayer PCB [11] instead of discrete magnetic cores. A similar approach can be used for capacitors, by stacking thin dielectric layers with high permittivity [12], but the capacitance density or voltage breakdown of such capacitors tend not to be suitable for power electronics [5].

Finally, it is also possible to embed standard Surface-Mount Devices (SMDs) [4], providing they are thin enough. This approach gives access to a very large catalog of components. In particular few integrated circuits are available in a bare die form that is compatible with direct embedding (which requires thick $\sim 10\mu\text{m}$ copper pads, with a relatively coarse pitch). Embedding packaged devices (or using an interposer between the chip and the PCB [13]) solves these problems, at the expense of a larger footprint. Multi-Layer Ceramic Capacitors (MLCCs) are another example of components which can be embedded, as they offer the capacitance values required in power electronics applications (micro-farads at several hundred volts).

The manufacturing technologies selected for our PFC converter are presented in the next section. Components were embedded in tests coupons, and then characterized to evaluate the consequences of the embedding process. The results are presented in section III. Finally, some test results of the complete converter are given in section IV and discussed in section V.

II. DESIGN AND MANUFACTURING PROCESS

The converter topology was chosen and optimized thanks to the procedures described in [14], [15]. This resulted in a PFC converter with 4 interleaved cells, each switching at 180 kHz, rated at 825 W, and based on SiC MOSFETs (CPM2-1200-0080B, Wolfspeed). The circuit diagram of this converter is presented in Fig. 1.

The actual implementation of the PFC stage in a structure based on PCB embedding is shown in Fig. 2. It is comprised of 3 separate boards, stacked together and separated with layers of Thermal Interface Material (TIM) (Sil-Pad 1500 ST, Bergquist). Because of their power density, and because they are directly connected using microvias, the semiconductor dies are embedded in a dedicated, thin PCB located close to a heatsink. The other (packaged) components are soldered

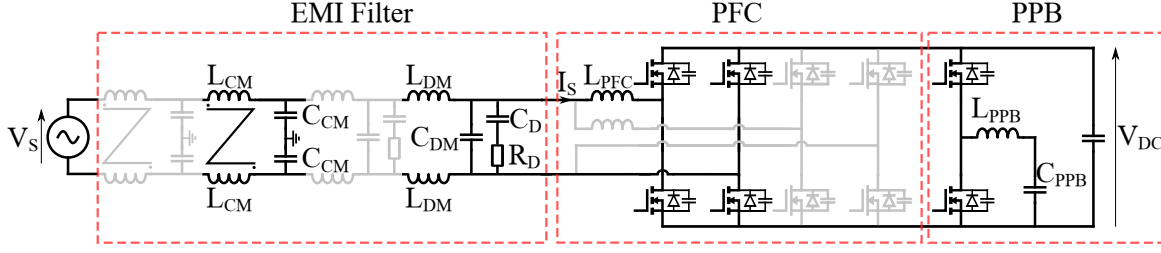


Fig. 1. Circuit diagram of the converter. Gray parts denote sections of the circuit which are duplicated: there are actually 3 common mode (CM) and differential mode (DM) stages for the EMI filter, and 4 PFC cells, each comprised of 4 MOSFET and inductor L_{PFC} . The Power Pulsating Buffer (PPB) stage intended for DC filtering is not addressed in this article.

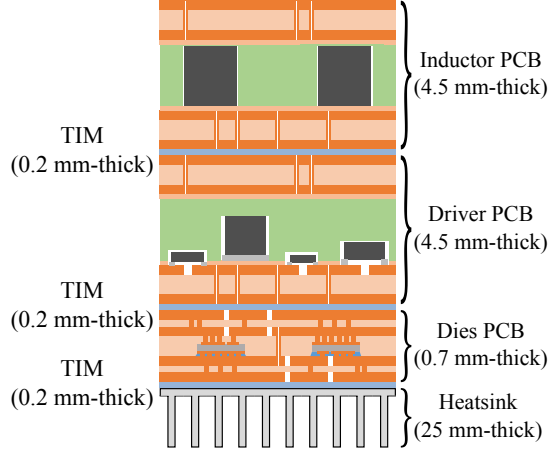


Fig. 2. Structure of a PFC cell, based on a stack of 3 PCBs and a heatsink

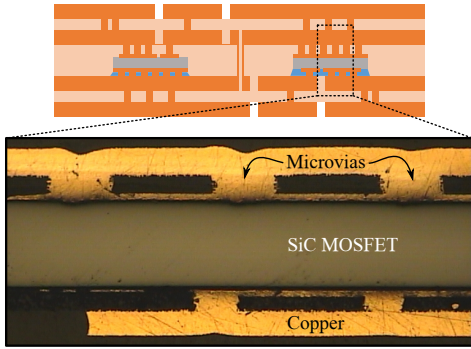


Fig. 3. Cross section of the "thin" board, showing the microvias connecting the SiC devices

onto inner layers of thicker PCBs. Magnetic cores are also embedded in thick PCBs. These can be placed further away from the heatsink, because of the lower power density they dissipate.

The embedding of the chips starts by gluing them onto a plain sheet of copper. Then, sheets of glass fiber impregnated with un-cured resin (prepregs) are stacked around the dies, followed by a second layer of copper. Vacuum lamination is then performed so that the resin flows to fill the voids and cures. Microvias are then drilled with a laser, and filled with copper to connect the drain, source and gate terminals of the MOSFETs. The copper layers are patterned using chemical etching to form the circuit layout. The microsection

of an embedded SiC MOSFET is given in Fig. 3. A second lamination cycle is performed to bond two additional copper layers and form a 4-layer PCB. This is required to route all the signals, but also for mechanical strength (a thin, 2-layer board would be too weak for proper handling) and thermal management (more copper layers improve heat spreading).

The thicker boards ("Driver" and "Inductor", in Fig. 2) are made simultaneously on the same panel, as they share the same stack-up configuration. The manufacturing starts with a thin, two-layer PCB (MCL-E-679, Hitachi), which is patterned according to the desired layout. A contour of solder resist is printed where components are to be mounted. Components are then assembled using a standard soldering process (stencil printing/automated positioning/solder reflow). A set of prepregs and cured glass-epoxy sheets are then machined and stacked to make-up for the thickness of the components and of the ferrite cores; a second two-layer board is placed on top (to form a symmetrical structure and prevent warpage); the stack is then laminated under vacuum and through-all vias are formed to interconnect the 4 copper layers.

III. CHARACTERIZATION OF THE TEST COUPONS

Several test coupons were made for each part used in the converter (all PCBs presented here were manufactured by Cimulec, France). This includes relatively large ceramic capacitors, diodes, or SiC MOSFETs. The characterization of these test coupons, along with that of some components of the converter which could also be tested individually (for example, the SiC dies, for which all three terminals can be accessed), is presented below.

A. SiC MOSFETs

An X-ray image of an embedded SiC MOSFET is given in Fig. 4. In this image, the microvias appear as darker dots. The outline of the die is highlighted with black lines for clarity sake. It shows satisfying alignment of the vias, especially on the gate contact ($500 \times 800 \mu\text{m}^2$).

The static characteristic of the MOSFET coupons was measured using an IWATSU CS-5400 curve tracer in 4-wire configuration. An example is given in Fig. 5. Overall, all 8 test coupons were characterized and showed similar characteristics. The main parameter, the on-state resistance ($R_{DS_{on}}$) of the coupons is presented in Fig. 6a. The values are consistent with the $R_{DS_{on}}$ quoted in the datasheet of the devices (80 mΩ,

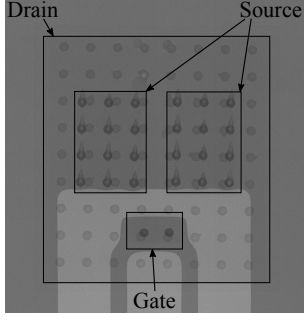


Fig. 4. X-Ray image of one of the embedded dies, showing the microvias used to contact the gate, drain and source terminals. Die size: $3.36 \times 3.1 \text{ mm}^2$.

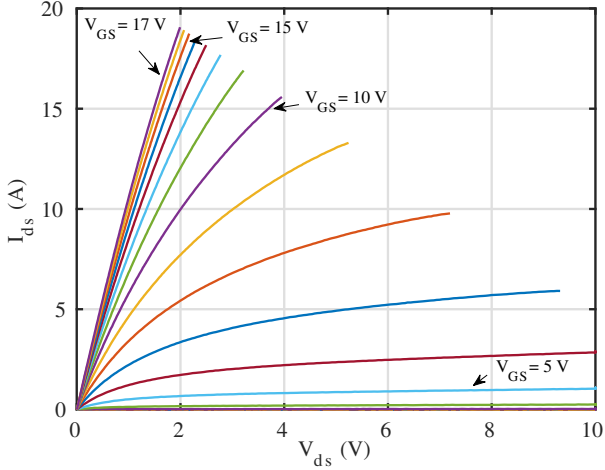


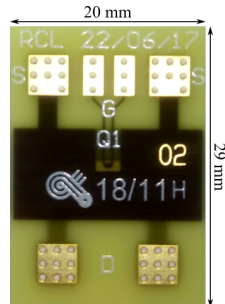
Fig. 5. Direct static characteristic of one of the SiC MOSFET coupons

[16]). Their slightly higher value can be associated with the interconnect resistance of the coupons (Fig. 6b), as the 4-wire measurement configuration is not maintained up to the SiC MOSFET. In the off state, the drain leakage current of the MOSFETs remains well below the limits specified by the manufacturer [16] ($1 \mu\text{A}$ at 1200 V typical, $100 \mu\text{A}$ max.), as shown in Fig. 7.

Other measurements were performed (using a Keithley 2636A SMU), on the 8 MOSFET coupons as well as on the 9 PFC boards (each containing 4 SiC chips), for a total of

Coupon	$R_{DS_{on}}$
#1	88.7 Ω
#2	77.9 Ω
#3	82.2 Ω
#4	83.3 Ω
#5	86.3 Ω
#6	89.1 Ω
#7	88.9 Ω
#8	84.2 Ω

(a)



(b)

Fig. 6. (a) $R_{DS_{on}}$ of the MOSFETs coupons. (b) photograph of one of the SiC MOSFET coupons.

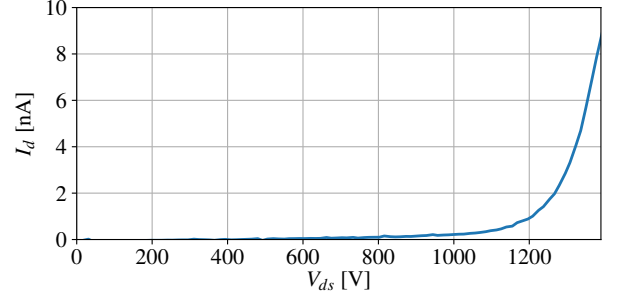


Fig. 7. Drain current in the off state ($V_{GS} = 0 \text{ V}$ through one of the embedded SiC MOSFETs, as a function of V_{DS} .

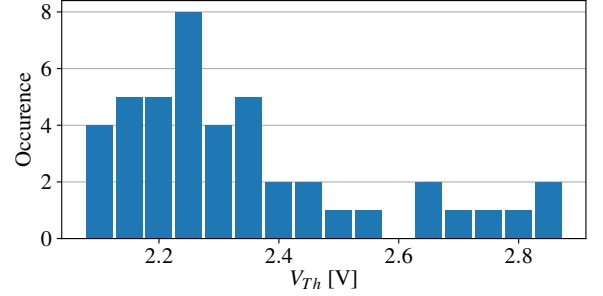


Fig. 8. Distribution of threshold voltages for 44 embedded SiC MOSFETs.

44 MOSFETs. Gate leakage current measurements were all found to be in the range of tens of pico-amperes, except for one device which has a gate leakage current of 250 nA at 20 V . The distribution of the threshold voltages (defined as the V_{GS} value required to reach a drain current of 5 mA under a V_{DS} of 5 V) is presented in Fig. 8, and is consistent with the datasheet of the devices.

Overall, no degradation of the MOSFETs was found after embedding, except possibly for one of the chips, which exhibited a higher (but still acceptable) leakage current.

B. SMD diodes

Three kind of SMD diodes are used in our gate driver circuit: two zener diodes (4.7 V and 15 V , On Semiconductor MMSZ52 series) for the regulation of the output voltage ($-5/15 \text{ V}$), and one 600 V fast rectifier for the bootstrap power supply (VS-1EFU06HM3, Vishay Semiconductors). This latter diode has the biggest package (a SMF case, roughly $2.9 \times 1.9 \times 1.1 \text{ mm}^3$), while the two zener diodes are slightly smaller (SOD 123 case, $2.7 \times 1.6 \times 1.2 \text{ mm}^3$).

Forward and reverse characterization results for 4 coupons of each diode reference are presented in Fig. 9. They show consistent characteristics, which match the manufacturer's specifications. One 600 V diode failed during the characterization, but no conclusion was reached regarding the possible causes of failure.

C. Ceramic capacitors

Ceramic capacitors were selected for embedding, as they can sustain the high temperatures associated with the PCB lamination process (above 180°C for 1-2 h). However, ceramic

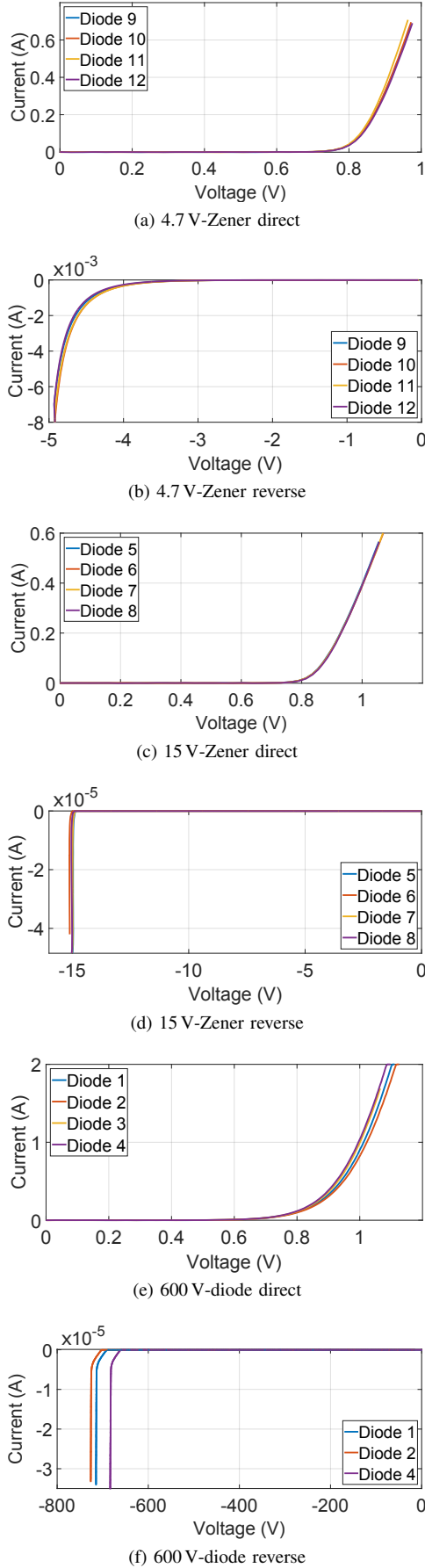


Fig. 9. Electrical characterization of the diodes used in the bootstrap power supply circuit for the gate driver. The forward and reverse characteristics of all tested diodes are in agreement with their datasheet.

TABLE I
LEAKAGE CURRENT OF 500 V CERAMIC CAPACITORS

Capacitor type	Leakage current (@500 V)
330 nF non embedded (ref)	107.0 nA
330 nF embedded (#1)	83.0 nA
330 nF embedded (#2)	96.0 nA
330 nF embedded (#3)	106.0 nA
56 pF non embedded (ref)	1.02 nA
56 pF embedded (#1)	2.64 nA
56 pF embedded (#2)	0.81 nA
56 pF embedded (#3)	0.86 nA

capacitors are brittle, and may crack when submitted to the lamination pressure. Cracks would then result in an increase in the leakage current in the capacitor.

An example of the leakage currents measured on the capacitor coupons is presented in Tab. I (using a Keithley 2410 SMU, after 15 min biasing). The 500 V, 330 nF X7R capacitors (C1812W334KCRCTU, Kemet, 1812-size case) are used for decoupling of the dc bus, while the C0G 56 pF capacitors (C1206C560JCGACTU, Kemet, 1206-size case) are connected in parallel with the output capacitance of the SiC MOSFETs for soft-switching operation. Other lower-voltage capacitors were also investigated (such as those used in the bootstrap power supply of the gate driver), but they are not presented here as they offer similar results.

Compared to the reference (an identical capacitor not connected or mounted to any board), there is no noticeable increase in leakage current for any embedded capacitor.

D. Inductors

Inductors are the bulkiest component in our converter, as the magnetic cores alone are 50 or 63 mm in diameter (for the EMI filter and the PFC inductor respectively, both with a thickness of 3 mm). X-Ray images of two inductors are shown in Fig. 10. While most of the cores were found to be in good condition, such as that presented in Fig. 10a, some were found to be broken (Fig. 10b), possibly because of the pressure experienced during the lamination process.

However, broken cores might only partially explain the characterization results presented in Fig. 11: a large discrepancy is found among the inductance values (from 10 to almost 100 μ H) and ac resistances exceed 10 Ω at the switching frequency of the PFC (180 kHz). This is an unacceptably high value for a converter cell rated at 825 W.

Several phenomenon seem to be involved in these disappointing results: the fringing magnetic field around the large airgap (Fig. 10a) induces strong eddy currents in the nearby copper windings [17]; broken and/or misaligned cores cause variations in the inductor behaviour; finally, current investigations seem to indicate that the inductor structure, with large, flat copper windings parallel to the core surface may intrinsically offer poor frequency performances.

IV. CHARACTERIZATION OF A PFC CELL

A photograph of a PFC cell is shown in Fig. 12. It corresponds to the structure shown in Fig. 2, with 3 stacked

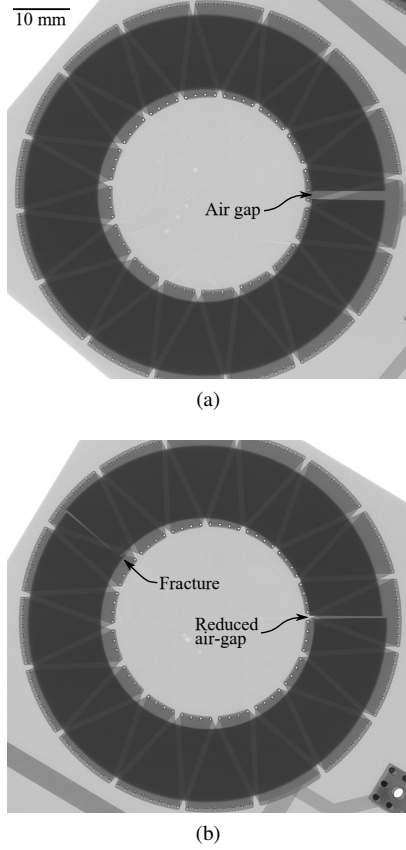


Fig. 10. X-ray images of two PFC inductors: (a) one in good condition and (b) one which cracked during lamination. Both magnetic cores are 63 mm in diameter, 3 mm-thick.

PCBs on top of a heatsink. 4 such cells are then assembled to form the interleaved PFC, as shown in Fig. 13a (in this case, electrolytic capacitors were used for testing instead of the PPB stage described in Fig. 1). Finally, the input EMI filter is presented in Fig. 13b.

As described in Section III, all components were found to operate satisfyingly after embedding, with the exception of the inductors. Therefore, it was possible to operate the converter, albeit at a limited power level. The current in the AC link of each PFC cell is shown in Fig. 14. While they exhibit satisfying sinus shapes, their amplitudes are noticeably different. This is because of the differences in inductor values described in section III-D. Replacing the embedded inductors with more standard planar inductors yielded a much better current balance, and allowed us to reach higher power levels. This is, however, beyond the scope of the present paper.

V. DISCUSSION AND CONCLUSION

Component embedding showed a very satisfying yield for a prototype run, with 43 SiC diodes out of 44 exhibiting good, consistent performances. The same conclusions were drawn for all the components, in particular regarding the gate drive board, which contains a few dozen components (a gate drive IC, a bootstrap power supply, some resistors and capacitors, as well as temperature sensors).

The main issue is related to the inductors, which are the largest component in the system. Even without considering the

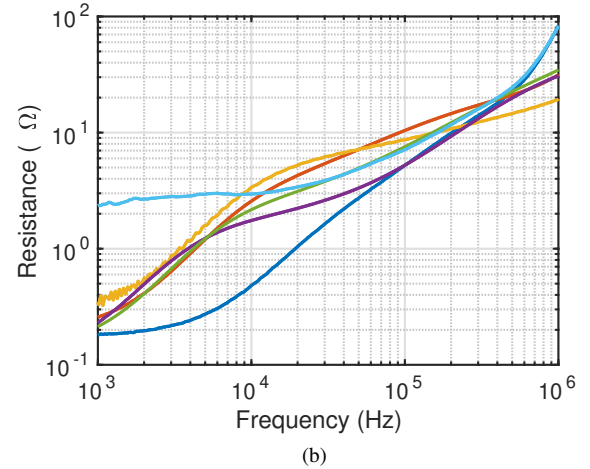
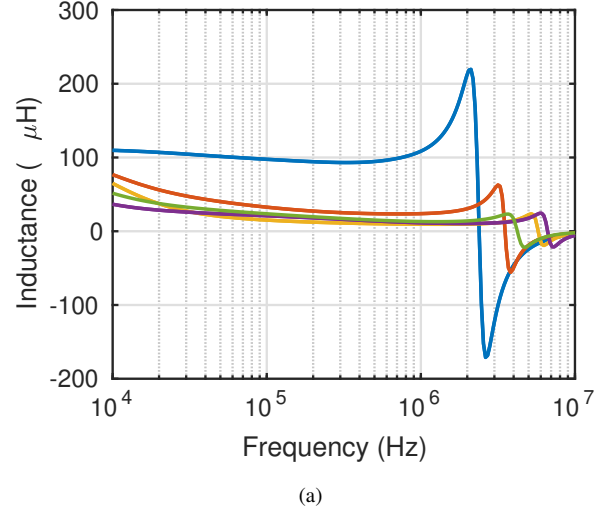


Fig. 11. Evolution of the inductance and of the resistance of the PFC inductors as a function of frequency, showing a dramatic increase in resistance and the discrepancy between supposedly identical inductors.

few of them that broke during the embedding (this should easily be solved in future manufacturing runs), the performance of these components is not yet satisfying. In particular, they exhibit a very large ac resistance at 180 kHz. It is not sure whether this can be reduced down to acceptable levels, even by removing the copper windings close to the air gap.

Another issue with the embedded inductors is their very flat form factor, which results in a flat EMI filter (Fig. 13b). While such a form factor might be desirable in a few cases (for example, in [10], the authors presented a flat flyback converter intended for supplying flat displays), it is not the case of most applications, where a more compact outline is preferred. Stacking PCBs is possible, as demonstrated with the PFC cells, but it requires extra care regarding thermal management. Also, embedding all components does not really save space (in our case, the volume of the PFC cells is 0.69 L and that of the EMI filter 0.16 L), as the thickness of the entire board is dictated by the thickest component. A more compact option probably includes embedding some components, while some other are mounted on the surface, in a more traditional manner.

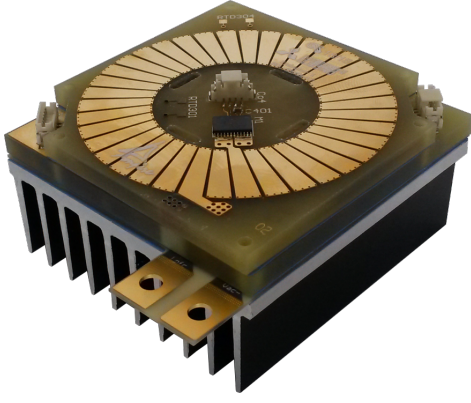
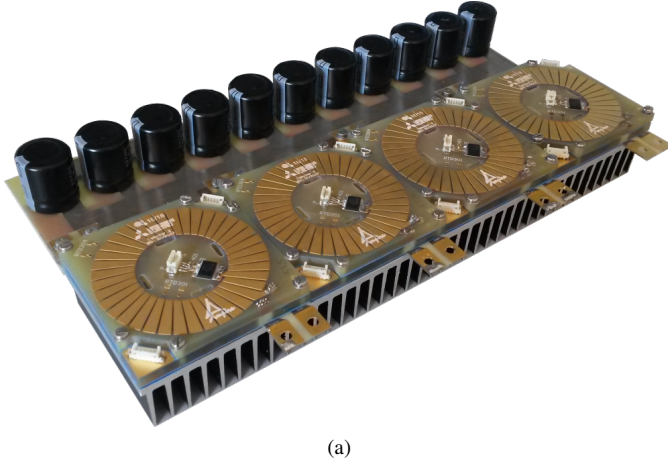
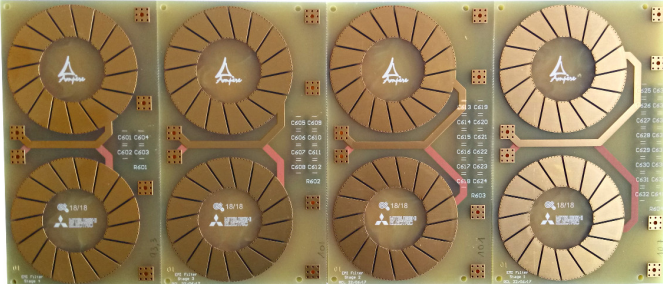


Fig. 12. Photograph of one PFC cell (size $7 \times 7 \times 3.5 \text{ cm}^3$).



(a)



(b)

Fig. 13. Photographs of (a): the 4 PFC cells ($28 \times 7 \times 5 \text{ cm}$) and (b): the input filter (4 LC stages, $28 \times 14 \times 0.4 \text{ cm}$).

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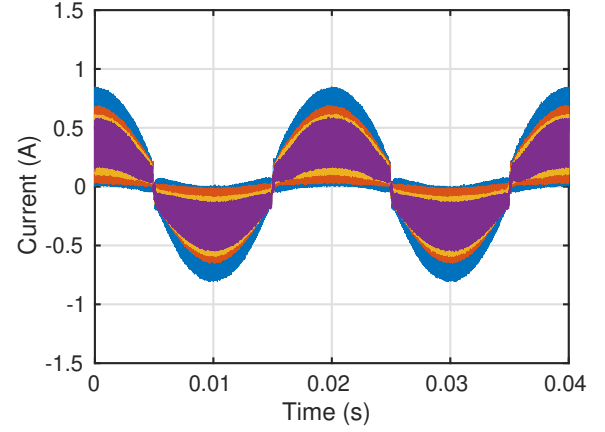


Fig. 14. Current in the 4 interleaved PFC cells, at low power.

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