Analysis and design of modular multilevel converters with partial integration of energy storage systems

Leandro de Oliveira Porto, Florian Errigo, Florent Morel

ANALYSIS AND DESIGN OF MODULAR MULTILEVEL CONVERTERS WITH PARTIAL INTEGRATION OF ENERGY STORAGE SYSTEMS

***Leandro D O Porto*[1], *Florian Errigo*[1]*, *Florent Morel*[1]**

[1] *SuperGrid Institute SAS, Villeurbanne, France*
**E-mail: florian.errigo@supergrid-institute.com*

Keywords: high-voltage direct current (HVDC), power converter, modular multilevel converter (MMC), energy storage system, frequency support

Abstract

With the massive integration of renewable energies, power converters will become increasingly important in the electrical grid of the future. One of the expected consequences is the reduction of system inertia. A promising alternative for this problem is the integration of energy storage elements (ESEs) into modular multilevel converters (MMCs). This paper presents a novel design methodology for a 3-phase MMC with partial integration of energy storage (MMC-PIES). The arms of the proposed converter contain standard submodules without energy storage (SMs) and submodules with an integrated ESE (ES-SMs). ES-SMs with half-bridge (HB) and full-bridge (FB) topologies are explored, while an HB configuration is kept for standard SMs. The methodology includes a minimisation of the amplitude of the circulating current that needs to be injected and a method to calculate the specifications of the converter. Like the results found in the literature, the proposed approach shows that using FB cells demands less ES-SMs. However, it is identified that the capacitances and ESEs must be remarkably bulkier, rendering this topology less attractive. The results also show that the partial integration with HB ES-SMs is a viable solution, causing only a small impact on the SM capacitance and on the ESEs rating.

1 Introduction

In the context of energy transition and the pursuit of carbon neutrality, the use of renewable energies is expected to quickly grow in the years to come. Renewable power plants integrated with power converters (for example, solar and most wind plants) cannot intrinsically contribute to the system inertia, since the converter decouples the generation unit from the grid [1]. This leads to stability issues since the grid frequency reacts more abruptly and suddenly in case of an imbalance between the generation and consumption of electricity.

Keeping this balance is part of the objective of the ancillary services required by Transmission System Operators (TSOs). Currently, primary, secondary and tertiary reserves are the main mechanisms for frequency control. However, their activation time is slow this is due to the inherent mechanical time constants of the machines. Therefore, the instantaneous inertial response is essential nowadays as it slows down the variation of the frequency until the reserves are fully operational.

In a scenario with reduced inertia level, new alternatives can be explored to provide a fast response during a short amount of time. For instance, the integration of energy storage systems (ESSs) into power converters has been highlighted in [2]–[5]. Modular topologies are remarkably suitable for this purpose. They offer an improved scalability and flexibility by splitting the energy storage elements (ESEs) between their modules. Thus, converters with integrated ESS can be used for the provision of ancillary services and frequency support.

More specifically, the partial integration of energy storage has been verified in [4], [5]. The motivation is to obtain a solution that is more cost-effective and smaller than a converter with a full integration of energy storage, i.e. with all submodules having an integrated ESE. To minimise the number of ESEs, the converters proposed in these works contain full-bridge (FB) submodules with integrated energy storage. Nevertheless, an in-depth analysis of the consequences of having partial integration on the required specifications of the converter (capacitances and switches, for example) has not been carried out.

This paper considers a 3-phase modular multilevel converter (MMC) with partial integration of energy storage (MMC-PIES). Each phase is composed of a lower and an upper arm that are strictly identical. Based on the works of [4], all arms have a mixed composition containing both standard submodules (SMs) without energy storage and energy storage submodules (ES-SMs) with an integrated ESE. While SMs have a half-bridge (HB) cell, the ES-SMs can have either an HB or an FB topology. The objective of this research is to analyse the feasibility and the attractiveness of the MMC-PIES with both topologies in comparison with an MMC with full integration of energy storage (MMC-FIES).

The paper is organised as follows. Section 2 details the diagram of an ES-SM and an MMC-PIES. In section 3, a design methodology for this converter is discussed. Then, an example of an MMC designed using the developed method is presented in section 4. This is followed by an analysis of the results of both topologies considered. A comparison with the MMC-FIES and with a standard MMC (with no integrated ESS) is also introduced, while section 5 concludes the advantages and drawbacks of such concept.

2 MMC with Partial Integration of Energy Storage

Fig 1 shows the diagram of the MMC-PIES. The total number of submodules in an arm (N) is the sum of the number of SMs (N_{SM}) and ES-SMs (N_{ES-SM}). The arm, DC and AC currents (I_{arm}, I_{DC} and I_{AC} respectively) are indicated alongside the DC and AC (RMS and phase-to-neutral) voltages (V_{DC} and V_{AC}). The arm and AC inductances, L_{arm} and L_{AC}, are also presented. The circulating current I_{circ} is internal to the converter, which means it has no impact on the DC and AC currents in steady state. Its use in the MMC-PIES is explained later. V_{ZS} is a zero-sequence voltage used to inject a third harmonic component in the voltage modulated by the MMC [7].

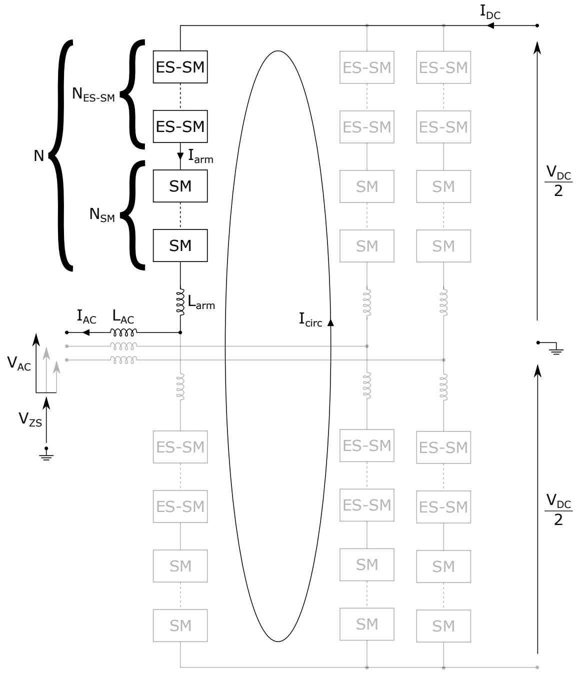

Fig. 1. Schematic of the considered MMC-PIES

By convention, if an MMC is working as an inverter, the AC and DC active powers (P_{AC} and P_{DC} respectively) that flow through the converter are positive. When it is operating as a rectifier, their values are negative. Therefore, a power imbalance ΔP can be defined by equation (1).

$$\Delta P = P_{AC} - P_{DC} \quad (1)$$

In a standard MMC with no integrated energy storage, ΔP must remain equal to zero to ensure the proper operation of the converter. When an ESS is available, this latter can be used to cover up an imbalance. If $\Delta P > 0$, the ESS supplies additional energy to the converter. Meanwhile, the ESS absorbs the excess energy when $\Delta P < 0$.

Fig 2 presents the configuration of an ES-SM with an HB topology. A DC-DC converter is included to decouple the ESE from the capacitor of the submodule. This prevents the use of oversized ESEs and a decreased performance [6]. Similarly, an ES-SM with an FB cell also has this converter.

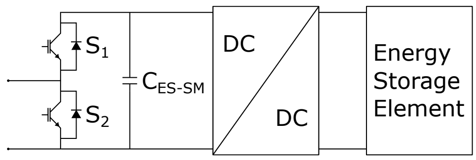

Fig. 2. Diagram of ES-SM with half-bridge topology

3 Design Methodology

The design methodology includes the calculation of the minimum number of ES-SMs required for a converter with a defined nominal power (without energy storage) P_{nom} and a maximum power imbalance ΔP_{max} that has to be compensated by the ESS. The method is also used to calculate the required SM and ES-SM capacitances, the minimum power of each ESE and the average, peak and RMS values of arm currents. The designed converter must be able to operate at all possible operating points, such as with reduced active power or increased reactive power Q_{AC}. In this paper, the reactive power requirement is considered to be up to $\pm 30\%$ of the active power.

Since all arms are identical, the design process can be focused only on one arm. To simplify the analysis, the voltages of the submodules are supposed to be correctly balanced. So, each arm can be represented as two voltage sources in series using an arm average modelling, as illustrated in Fig 3 for an upper arm. V_{SM} and V_{ES-SM} are the voltage sources representing the SM and ES-SM stacks respectively. The total modulated voltage V_{mod} is the sum of V_{SM} and V_{ES-SM}.

It can be noted that the arm current has an AC and a DC component, as indicated in equation (2) for an upper arm.

$$\begin{aligned} I_{arm}(t) &= \frac{I_{DC}}{3} + \frac{I_{AC}(t)}{2} + I_{circ}(t) \\ &= \frac{P_{DC}}{3V_{DC}} + \frac{\sqrt{2}P_{AC}}{6V_{AC}\cos(\phi)}\sin(\omega t - \phi) + I_{circ}(t) \end{aligned} \quad (2)$$

Similarly, V_{mod} also has AC and DC components. However, two extra terms must be added to prevent a distortion of V_{AC} caused by the arm and AC inductances as in (3). It can be noted that V_{ZS} is also included to modulate the injection of the zero-sequence voltage.

$$\begin{aligned} V_{mod}(t) = &\frac{V_{DC}}{2} - \sqrt{2}V_{AC}\sin(\omega t) - V_{ZS}(t) \\ &-L_{arm}\frac{dI_{arm}(t)}{dt} - L_{AC}\frac{dI_{AC}(t)}{dt} \end{aligned} \quad (3)$$

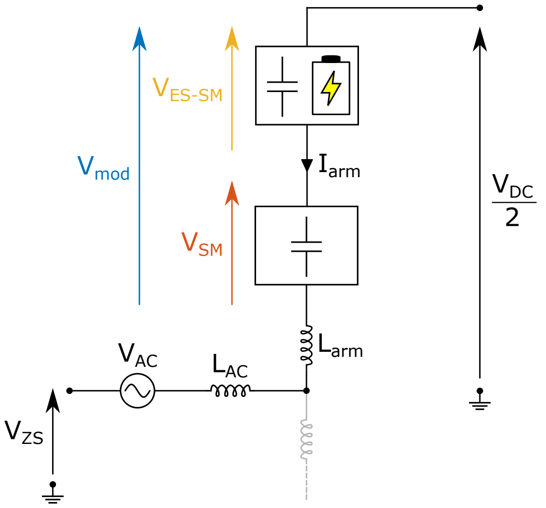

Fig. 3 Equivalent voltage source model of an upper arm of the MMC-PIES

3.1 Voltage modulated by the submodules

In steady state, the voltage of a capacitor of a submodule must have a constant average value to ensure the proper operation of the converter. The voltage of a capacitive device is linked to its stored energy. Therefore, the average voltage will remain constant if the average energy is constant.

This means that the energy deviation of the voltage source representing the stack of SMs ΔE_{SM} at the end of each cycle must be equal to zero [4]. This is indicated by equation (4), where T is the period of a cycle.

$$\Delta E_{SM}(T) = \int_0^T V_{SM}(t) * I_{arm}(t)\, dt = 0 \quad (4)$$

The ES-SM voltage must be precisely calculated to meet this condition. The energy deviation of the voltage source of the ES-SMs ΔE_{ES-SM} should then be equal to the energy deviation of the arm ΔE_{arm}, as in (5).

$$\int_0^T V_{ES-SM}(t) * I_{arm}(t)\, dt = \int_0^T V_{mod}(t) * I_{arm}(t)\, dt = T * \Delta P/6 \quad (5)$$

An analytical method to calculate the ES-SM voltage is proposed in [4]. It depends on the topology chosen for the ES-SMs. If FB is being used, the ES-SM voltage has a constant absolute value with a sign that changes with time depending on the sign of $I_{arm}(t)$ and ΔP. For example, if I_{arm} and ΔP are positive, the ES-SM voltage is negative. This is necessary to ensure the power that is being exchanged has the correct sign.

Nevertheless, HB submodules cannot generate a negative voltage. Therefore, if HB ES-SMs are used, their voltages are different from zero only when the sign of $I_{arm}(t)$ is different from the sign of ΔP. During these time intervals, the ES-SM voltage is constant and positive.

A numerical method is also introduced in [4] to take into consideration realistic constraints on the SM voltage. Based on this, an adapted method is proposed in this paper. The most important modification is that the maximum voltage of SM capacitors is now considered constant during the design process. Consequently, the SM capacitance does not need to be pre-defined as in the original work. Instead, it can be minimised while respecting a maximum voltage deviation constraint, which is detailed later. This prevents the use of oversized capacitors, rendering the solution more attractive.

Finally, the number of submodules with integrated energy storage can be calculated as in (6), with $\overline{V_C}$ being the average voltage of a submodule and ΔV_{pu} the maximum voltage deviation of the capacitors.

$$N_{ES-SM} = \text{ceil}\left(\frac{\max(|V_{ES-SM}(t)|)}{(1-\Delta V_{pu})\overline{V_C}}\right) \quad (6)$$

3.2 Injection of circulating current

The designed MMC-PIES must operate correctly if the active power is reduced. In that case, the amplitude and the DC offset of the arm current are reduced too. However, the arm energy deviation at the end of a period is only a function of ΔP and T, as indicated in equation (5).

So, for a fixed ΔP, the ES-SM stack has to reach the same energy deviation independently of the active power level. When I_{arm} is reduced, the ES-SM voltage must be inherently increased. Consequently, the number of ES-SMs required is higher. When all operating points are considered, the conclusion is that all submodules of the MMC-PIES must have an ESE [4]. This would mean that the proposed converter with mixed arms is not feasible.

In order to increase the arm current without affecting the DC and AC currents, a solution consists in injecting a second harmonic circulating current as proposed in [4]. In this approach, I_{circ} is maximised in order to minimise as much as possible the required number of ES-SMs during the operation at reduced power level.

It was observed that this circulating current had a big impact on the amplitude of the energy deviations of the submodule capacitors. Consequently, the required SM and ES-SM capacitances values were significantly high, resulting in a solution with bulkier submodules. Therefore, a new approach to minimise the amplitude of this current is proposed below.

A second harmonic circulating current is chosen. It is defined as in (7). $\widehat{I}_{circ}$ is its amplitude and ψ_{circ} is the phase shift between I_{circ} and the fundamental current of the arm I_{fund} (composed of the DC and grid frequency terms in equation (2)). Equation (8) shows the values of ψ_{circ}.

$$I_{circ} = \widehat{I}_{circ} \sin(2(\omega t - \phi + \psi_{circ})) \quad (7)$$

$$\psi_{circ} = \begin{cases} \pi/4, & \text{if } P_{DC} \geq 0 \\ -\pi/4, & \text{otherwise} \end{cases} \quad (8)$$

The number of ES-SMs is calculated only for the operating point with maximum amplitude of the arm current when no I_{circ} is injected. This happens for $P_{DC} = P_{nom}$, $P_{AC} =$

$P_{nom} + \Delta P_{max}$ and maximum Q_{AC}. For all other operating points, it is possible to find the minimum amplitude of I_{circ} that reduces the necessary number of ES-SMs to be equal to the value calculated in the reference point above. This is done by setting the ES-SM voltage to be as high as possible and then iteratively adjusting the value of $\widehat{I}_{circ}$. This is repeated until the energy deviation of the SMs is sufficiently close to zero. By doing this, $\widehat{I}_{circ}$ is minimised while ensuring that no additional ES-SMs are required for operation at reduced power level.

3.3 Calculation of the capacitances

As mentioned, the SM and ES-SM capacitors need to be kept at a constant average voltage to ensure the proper operation of the MMC. Nevertheless, their voltages fluctuate due to the intrinsic changes in their energy. This variation around the average value must be limited.

If the voltage gets too low for some moments, the converter would not have enough voltage available to modulate the arm voltage. If the voltage gets too high, the capacitors would be overcharging. This can speed up their ageing process or damage them [8]. The submodules switches could also be damaged. Therefore, the maximum voltage deviation ΔV_{pu} is defined.

3.3.1 Submodules without energy storage: A method is presented in [8] to calculate the capacitance of a standard MMC submodule (with no integrated ESE). First, the energy of the stack of capacitors of the SMs, $\Delta E_{stack_{SM}}$, is calculated for any time t as in equation (9). The variable x is introduced just to avoid any confusion with the upper limit of integration t. It can be noted that the energy deviation of the stack of capacitors is equal to the energy deviation of the SM voltage source ΔE_{SM}.

$$\Delta E_{stack_{SM}}(t) = \Delta E_{SM}(t) = \int_0^t V_{SM}(x) * I_{arm}(x)\, dx \quad (9)$$

Finally, the capacitance of a standard SM, C_{SM}, can be calculated with equation (10), where $\Delta E^{pk-pk}_{stack_{SM}}$ is the peak-to-peak amplitude of $\Delta E_{stack_{SM}}$.

$$C_{SM} = \frac{\Delta E^{pk-pk}_{stack_{SM}}}{2N_{SM}\overline{V_C}^2 \Delta V_{pu}} \quad (10)$$

Therefore, the required SM capacitance is calculated for all possible operating points of the converter. The highest value is then chosen as the final value of C_{SM}.

3.3.2 Submodules with energy storage: When there is an imbalance between the AC and DC sides of the MMC, there is an energy exchange between the capacitors of ES-SMs and the ESEs. Thus, this additional energy ΔE_{ESE} needs to be considered in the calculation of the energy deviation of the ES-SM stack of capacitors $\Delta E_{stack_{ES-SM}}$. So, an adaptation of the method in [8] was developed to calculate the capacitance of an ES-SM. Equation (11) presents the equation of $\Delta E_{stack_{ES-SM}}$.

$$\Delta E_{stack_{ES-SM}}(t) = \Delta E_{ES-SM}(t) + \Delta E_{ESE}(t) \quad (11)$$

The energy exchanged with the ESEs depends on the control of the energy storage system. Supposing a constant exchange of power, ΔE_{ESE} is defined as in (12). The division by 6 is necessary because the required energy is equally divided between all six arms of the converter.

$$\Delta E_{ESE}(t) = t * \Delta P/6 \quad (12)$$

The capacitance of an ES-SM C_{ES-SM} can be then calculated as in (13), where $\Delta E^{pk-pk}_{stack_{ES-SM}}$ is the peak-to-peak value of $\Delta E_{stack_{ES-SM}}$. As in the case of standard SMs, the worst-case scenario is considered for the final value of C_{ES-SM}.

$$C_{ES-SM} = \frac{\Delta E^{pk-pk}_{stack_{ES-SM}}}{2N_{ES-SM}\overline{V_C}^2 \Delta V_{pu}} \quad (13)$$

3.4 Power of an energy storage element

The ESEs must be designed according to the maximum instantaneous power P^{max}_{ESE} that each one needs to supply. It depends on the number of ES-SMs, as the required power is supposed to be equally divided between all ESEs. Therefore, P^{max}_{ESE} is calculated with equation (14).

$$P^{max}_{ESE} = \frac{\Delta P_{max}}{6N_{ES-SM}} \quad (14)$$

3.5 Submodule switches

The design of the submodule switches is defined by the current that flows through them. The current of a switch depends on its state (bypassed or inserted), so it is not equal to the arm current. Nevertheless, the arm current is analysed for the sake of simplicity. Three values must be rated for the worst-case scenario:

- Peak current I^{peak}_{arm}
- RMS current I^{RMS}_{arm}
- Average current I^{avg}_{arm}

These values can be then compared to the MMC-FIES and standard MMC cases. Therefore, it can be concluded if whether or not the same switches may be used for partial integration.

3.6 Volume of the submodules

One of the main motivations of a converter with partial integration of energy storage is to have a solution that is potentially less bulky than an MMC-FIES. After designing the MMC-PIES, an estimation of the volume of its submodules can be carried out to verify whether or not the size of the converter is reduced. The total volume of the ESEs is considered to be equal in both cases because their stored energy remains the same.

The capacitor usually stands for the majority of the total volume of a submodule [9]. Although calculating the volume can be complex, the maximum energy stored in the capacitors is a good indicator. By comparing this parameter for the MMC-PIES and the MMC-FIES, it is possible to obtain a relative estimation of their volume.

The maximum energy stored in the capacitors of an arm of the MMC with integration of energy storage $E_{C_{MMC}}^{max}$ is defined as in (15).

$$E_{C_{MMC}}^{max} = N_{SM} E_{C_{SM}}^{max} + N_{ES-SM} E_{C_{ES-SM}}^{max} \quad (15)$$

As a consequence of the way the capacitors were designed, the maximum voltage they reach in the worst-case scenario is $(1 + \Delta V_{pu})\overline{V_C}$. Therefore, $E_{C_{MMC}}^{max}$ can be calculated as shown in equation (16).

$$E_{C_{MMC}}^{max} = \frac{((1 + \Delta V_{pu})\overline{V_C})^2}{2}(N_{SM} C_{SM} + N_{ES-SM} C_{ES-SM}) \quad (16)$$

4 Results

The design methodology of the MMC-PIES was developed in MATLAB/Simulink. As an example, a case study is presented. Table 1 gives the parameters used in this analysis.

Table 1 Parameters selected for the case study of the design of an MMC-PIES

P_{nom}	Converter nominal power	1 GW
ΔP_{max}	Maximum power imbalance	0.1 GW
V_{DC}	DC pole-to-pole voltage	640 kV
V_{AC}	RMS and phase-to-neutral AC voltage	222 kV
f	Frequency	50 Hz
N	Number of submodules in each arm	200
$\overline{V_C}$	Nominal voltage of a submodule	3.5 kV
ΔV_{pu}	Maximum voltage deviation of a capacitor	0.1 pu
L_{AC}	AC inductance	50 mH
L_{arm}	Arm inductance	50 mH

The results obtained for the MMC-PIES with HB ES-SMs and with FB ES-SMs are shown in Table 2. Due to not being able to generate negative voltages, and thus requiring a higher positive voltage, the use of HB ES-SMs leads to an increased number of submodules with energy storage. 16.5% of the submodules must have an ESE. This number is only 3.5% if FB ES-SMs are used. These results are consistent with those presented in the literature [4], [5].

This could be seen as an advantage for the FB topology, but this is counterbalanced by having ESEs with a higher power requirement. They are consequently bulkier and more expensive when compared to the case with HB submodules. Moreover, it can be noted that bigger capacitances are also necessary for the use of FB cells. For example, the ES-SM capacitance is almost 50% lower in the case with HB ES-SMs.

To evaluate the attractiveness of the MMC-PIES, the results for an MMC-FIES with HB ES-SMs are also presented in Table 2. The specifications of a standard MMC with $P_{nom} = 1.1$ GW and $\Delta P_{max} = 0$ are available too.

The maximum energy stored in the capacitor is increased by 67.4% when comparing the MMC-PIES with FB ES-SMs with the MMC-FIES. This indicates that the volume occupied by the submodules of the converter is remarkably higher with this solution. This is a consequence of the high capacitances that are necessary with this topology. One of the expected benefits of partial integration was to have a smaller solution, which is not the case in this example. So, this can be seen as a heavy drawback for the MMC-PIES with FB ES-SMs.

The impact on the volume is less accentuated for the MMC-PIES with HB ES-SMs. The total energy stored in the capacitors is only 8.3% bigger than in the full integration case. Moreover, it is 14% higher than the standard MMC. Although this is not what was expected initially, the MMC-PIES with HB ES-SMs still has satisfactory advantages. The reduced number of ES-SMs and ES-SM capacitance render this converter viable when compared with the MMC-FIES.

The analysis of the arm current shows that the three rated values are independent of the solution. In all four cases, I_{arm}^{peak} is equal to 1.79 kA, I_{arm}^{RMS} to 1.04 kA and I_{arm}^{avg} to 0.57 kA. This means that the partial integration of energy storage has no impact on the rating of the switches.

Finally, the design of the MMC-PIES is validated with simulations in Simulink. Supposing that the voltages of all submodules are correctly balanced, an arm average model is used. Fig 4 shows an example of waveforms during one cycle of the converter with HB ES-SMs.

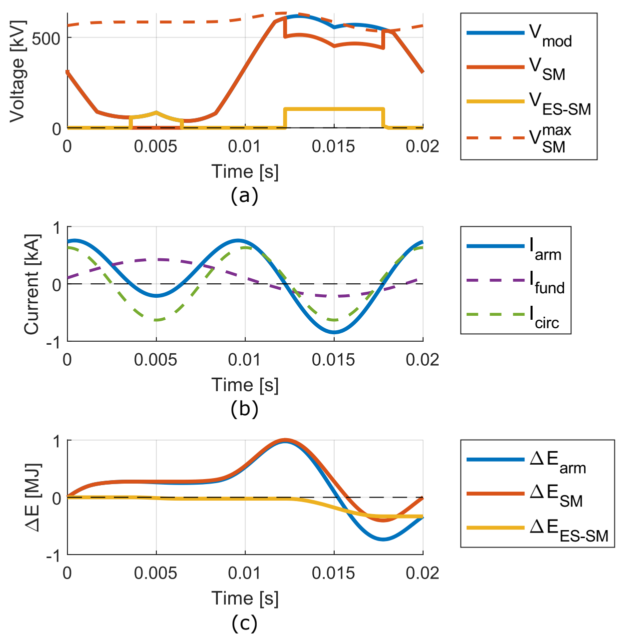

Fig. 4 Waveforms of the designed MMC-PIES with HB ES-SMs for $P_{DC} = 0.2$ GW, $P_{AC} = 0.3$ GW and $Q_{AC} = 0$:
(a) modulated, SM and ES-SM voltages
(b) arm, fundamental and circulating currents
(c) arm, SM and ES-SM energy deviations

Table 2 Specifications of the MMC-PIES, MMC-FIES and standard MMC for the parameters of the case study

	MMC-PIES with HB ES-SMs	MMC-PIES with FB ES-SMs	MMC-FIES with HB ES-SMs	Standard MMC with HB SMs
Proportion of ES-SMs	16.5%	3.5%	100%	0%
SM capacitance	4.06 mF	6.02 mF	-	3.42 mF
ES-SM capacitance	3.05 mF	6.06 mF	3.60 mF	-
Power of each ESE	0.51 MW	2.38 MW	0.08 MW	-
Total energy stored in capacitors	5.77 MJ	8.92 MJ	5.33 MJ	5.06 MJ

As stated in section 3.1, the voltage of the ES-SMs is different from zero only when the arm current has the correct sign (i.e. negative in this example), as seen in Fig 4a. The influence of the circulating current can be observed in Fig 4b. If it was not injected, the arm current would be equal to the fundamental current (purple dotted line) and a higher ES-SM voltage level would be necessary. Finally, it can be noted in Fig 4c that the energy deviation of the SMs is equal to zero at the end of the cycle as required.

5 Conclusion

This paper analyses a modular multilevel converter with partial integration of energy storage. Previous works in the literature focused on the use of energy storage submodules with a full-bridge topology, as less energy storage elements are necessary in this case. However, a verification of the impacts on other aspects of the converter has not been thoroughly done before.

A design methodology is proposed to investigate this. It includes a set of equations to calculate the SM and ES-SM capacitances for a maximum voltage deviation. Moreover, the specifications of the ESEs and switches are also inspected. An estimation of the volume of the submodules is carried out. The injection of circulating current is necessary for operation at reduced power level. As it has a big impact on the required capacitances, a iterative method to minimise its amplitude was developed. To validate the proposed method, simulations were carried out.

It was demonstrated that the MMC-PIES with FB ES-SMs does not seem to be a viable option. Although the low number of ES-SMs that are required, the high capacitances and ESE power strongly weigh against it. Consequently, it is shown that this solution would be notably bulkier than an MMC with full integration of energy storage. On the other hand, the MMC-PIES with HB ES-SMs could be a promising solution. The required number of energy storage elements can be greatly reduced while having a minor impact on the capacitances and on the volume of the submodules.

6 Acknowledgements

This work was supported by a grant overseen by the French National Research Agency (ANR) as part of the “Investissements d’Avenir” Program (ANE-ITE-002-01).

References

[1] Fernández-Guillamón, A., Gómez-Lázaro, E., Muljadi, E., et al.: ‘Power systems with high renewable energy sources: A review of inertia and frequency control strategies over time’, Renewable and Sustainable Energy Reviews, 2019, 115, 109369

[2] Schroeder, M., Henninger, S., Jaeger, J., et al.: ‘Integration of batteries into a modular multilevel converter’. 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, 2013

[3] Trintis, I., Munk-Nielsen, S., Teodorescu, R.: ‘Cascaded H-bridge with bidirectional boost converters for energy storage’. 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 2011

[4] Judge, P.D., Green, T.C.: ‘Modular Multilevel Converter With Partially Rated Integrated Energy Storage Suitable for Frequency Support and Ancillary Service Provision’, IEEE Transactions on Power Delivery, 2019, 34, (1), pp. 208-219

[5] Richter, M., Klein, K., Luther, M.: ‘Validation of a Modular Multilevel Converter with additionally integrated Energy Storage for Grid-supportive Operation’. 2020 6th IEEE International Energy Conference (ENERGYCon), Gammarth, Tunisia, 2020

[6] Errigo, F., Morel, F., Mathieu de Vienne, C., et al.: ‘A Submodule with Integrated Supercapacitors for HVDC-MMC providing Fast Frequency Response’, IEEE Transactions on Power Delivery, 2021

[7] Li, R., Williams, B.W., Fletcher, J.E.: ‘Influence of Third Harmonic Injection on MMC-based HVDC Transmission Systems’, IET Generation, Transmission & Distribution, 2016, 10, (11)

[8] Merlin, M., Green, T.: ‘Cell capacitor sizing in multilevel converters: Cases of the modular multilevel converter and alternate arm converter’, IET Power Electronics, 2015, 8, (3), pp. 350-360

[9] Tang, Y., Chen, M., Ran, L.: ‘A Compact MMC Submodule Structure With Reduced Capacitor Size Using the Stacked Switched Capacitor Architecture’, IEEE Transactions on Power Electronics, 2016, 31, (10), pp. 6920-6936